

What is claimed is:

1. A dual-bit nitride read only memory cell with
2 parasitic amplifier, comprising:
3 a semiconductor substrate;
4 a first well region disposed in the semiconductor
5 substrate and having a first conductive type
6 opposite to the semiconductor substrate;
7 a second well region disposed in the first well
8 region and having a second conductive type
9 opposite to the first well region;
10 a gate dielectric layer disposed over portions of
11 the second well region, wherein the gate
12 dielectric layer comprises a nitride layer;
13 a conductive layer disposed on the gate dielectric
14 layer to form a gate; and
15 a pair of first doped regions symmetrically disposed
16 in the second well region on both sides of the
17 gate and having a third conductive type
18 opposite to the second well region, wherein one
19 of the first doped regions, the second well
20 region and the first well region constitute a
21 parasitic current amplifier.

1 2. The nitride read only memory cell as claimed in
2 claim 1, wherein the semiconductor substrate is a P-type
3 silicon substrate.

1 3. The nitride read only memory cell as claimed in
2 claim 1, wherein the conductive layer is comprised of
3 polysilicon.

1 4. The nitride read only memory cell as claimed in
2 claim 1, wherein the first doped regions are N-type doped
3 regions having a doping concentration between $1*10^{19}$ and
4 $1*10^{21}$ atoms/cm².

1 5. The nitride read only memory cell as claimed in
2 claim 1, further comprising a pair of second doped
3 regions symmetrically disposed in the first well region
4 on both sides of the gate.

1 6. The nitride read only memory cell as claimed in
2 claim 5, wherein the second doped regions are N-type
3 doped regions having a doping concentration between $1*10^{19}$
4 and $1*10^{21}$ atoms/cm².

1 7. The nitride read only memory cell as claimed in
2 claim 1, wherein the parasitic current amplifier is a
3 bipolar junction transistor (BJT) including an emitter
4 constituted of one of the first doped regions, a base
5 constituted of the second well region and a collector
6 constituted of the first well region.

1 8. The nitride read only memory cell as claimed in
2 claim 1, wherein the gate dielectric layer is oxide-
3 nitride-oxide (ONO) layer.

1 9. A method of fabricating a dual-bit nitride read
2 only memory cell, comprising the steps of:
3 providing a semiconductor substrate;
4 forming a first well region in the semiconductor
5 substrate, and the first well region having a

6 first conductive type opposite to the
7 semiconductor substrate;
8 forming a second well region in the first well
9 region, and the second well region having a
10 second conductive type opposite to the first
11 well region;
12 sequentially forming a dielectric layer and a
13 conductive layer over the second well region to
14 form a gate thereon, wherein the dielectric
15 layer comprises a nitride layer; and
16 symmetrically forming a pair of first doped regions
17 in the second well region on both sides of the
18 gate, and the first doped regions having a
19 third conductive type opposite to the second
20 well region, wherein one of the first doped
21 regions, the second well region and the first
22 well region constitute a parasitic current
23 amplifier.

1 10. The method as claimed in claim 9, wherein the
2 dielectric layer is an oxide-nitride-oxide layer.

1 11. The method as claimed in claim 9, wherein the
2 first doped regions are N-type doped regions having a
3 doping concentration between 1×10^{19} and 1×10^{21} atoms/cm².

1 12. The method as claimed in claim 9, further
2 comprising the step of symmetrically forming a pair of
3 second doped regions in the first well region on both
4 sides of the gate.

1 13. The method as claimed in claim 12, wherein the
2 second doped regions are N-type doped regions having a
3 doping concentration between 1×10^{19} and 1×10^{21} atoms/cm².

1 14. The method as claimed in claim 9, wherein the
2 semiconductor substrate is a P-type silicon substrate.

1 15. The method as claimed in claim 9, wherein the
2 conductive layer is comprised of polysilicon.

1 16. The method as claimed in claim 9, wherein the
2 parasitic amplifier is a bipolar junction transistor
3 (BJT) including an emitter constituted of one of the
4 first doped regions, a base constituted of the second
5 well region and a collector constituted of the first well
6 region.

1 17. A method of reading a dual-bit nitride read
2 only memory cell constituted of a semiconductor
3 substrate, a first well region having a first conductive
4 type opposite to the substrate disposed in the substrate,
5 a second well region having a second conductive type
6 opposite to the first well region disposed in the first
7 well region, a gate dielectric layer comprising a nitride
8 layer disposed over portions of the second well region,
9 a conductive layer disposed on the gate dielectric layer
10 to form a gate, and a pair of first doped regions
11 symmetrically having a third conductive type opposite to
12 the second well region disposed in the second well region
13 on both sides of the gate, wherein one of the first doped
14 regions, the second well region and the first well region

15 constitutes a parasitic current amplifier, comprising the
16 steps of:

17 selecting a reading bit of the dual-bit nitride read
18 only memory cell, floating the gate and
19 grounding one of the first doped region on the
20 opposite side thereof;

21 applying a first voltage to the other first doped
22 region adjacent to the reading bit to generate
23 a leakage current into the second well region;

24 applying a second voltage to the first well region
25 on the opposite side of the reading bit to turn
26 on the current amplifier therein and amplify
27 the leakage currents; and

28 measuring an amplified current from the first well
29 region on the opposite side of the reading bit
30 to acquire the memory status of the reading
31 bit.

1 18. The method as claimed in claim 17, wherein the
2 reading bit is 0 when the amplified current is less than
3 $10^{-2} \mu\text{A}$.

1 19. The method as claimed in claim 17, wherein the
2 reading bit is 1 when the amplified current exceeds or
3 equal to $10^{-2} \mu\text{A}$.

1 20. The method as claimed in claim 17, wherein the
2 first voltage is between 1 and 10 volts.

1 21. The method as claimed in claim 17, wherein the
2 second voltage is between 1 and 10 volts.

1 22. The method as claimed in claim 17, wherein the
2 parasitic current amplifier has a current gain about 1
3 fold to 100 folds.

1 23. The method as claimed in claim 17, wherein the
2 leakage currents are gate-induced drain leakages (GIDL).

3 24. The method as claimed in claim 17, wherein the
4 second voltage is applied to a second doped region in the
5 first well region on the opposite side of the reading
6 bit.

1 25. The method as claimed in claim 24, wherein the
2 second doped region is N-type doped region having a
3 doping concentration between 1×10^{19} and 1×10^{21} atoms/cm².